CLAIMS

1. A data storage device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of cross points formed by the word lines and the bit lines;

a plurality of memory cells, each of the memory cells being located at a different one of the cross points; and

a first bit line comprising a distributed series diode along a length of the bit line such that each of the associated memory cells located along the first bit line is coupled between the distributed series diode and an associated word line.

2. The data storage device of claim 1, wherein the distributed series diode comprises a metal layer, a semi-conductor layer, and a material layer disposed between the metal layer and the semi-conductor layer.

3. The data storage device of claim 1, wherein each of the bit lines comprises a distributed series diode.

4. The data storage device of claim 1, wherein the distributed series diode has a defined lateral resistance per unit length, thereby allowing a first group of memory elements to be selectively isolated from remaining memory elements along the first bit line.

5. The data storage device of claim 4, wherein the first group of memory elements further comprises a selected memory element and the selected memory element is disposed between the first bit line and a first word line.

6. The data storage device of claim 1, further comprising a plurality of read circuits, wherein each read circuit is coupled to at least one bit line and is configured to sense current flow through a selected memory element.

7. The data storage device of claim 6, wherein each read circuit comprises a differential amplifier.

8. The data storage device of claim 7, wherein the differential amplifier is a current mode differential amplifier.

9. The data storage device of claim 8, wherein the differential amplifier is operable to compare current flowing through the selected memory element with current flowing through at least one reference memory element.

10. The data storage device of claim 8, further comprising multiple comparator circuits, each comparator circuit coupled to an associated read circuit and operable to convert an analog differential sense voltage to a digital output read signal.

11. The data storage device of claim 1, further comprising an equipotential generator coupled to the word lines and the bit lines and operable to set voltage levels in the data storage device to prevent parasitic currents from flowing through unselected memory cells.

12. The data storage device of claim 11, wherein the equipotential generator is configured to apply a potential to the first bit line, the potential relating to feedback from unselected word lines.

13. The data storage device of claim 12, wherein unselected word lines in a selected group of word lines are connected together to set an averaged feedback voltage that is approximately equal to an applied array voltage.

14. The data storage device of claim 13, wherein the equipotential generator is operable to establish equipotential isolation of a selected word line based upon feedback from one or more unselected word lines.

15. A method for forming a data storage device, comprising:

forming a plurality of word lines in a first plane;

forming a plurality of memory elements on the plurality of word lines; and

forming a plurality of bit lines, each bit line being a distributed series diode, the plurality of bit lines being disposed in a second plane that is substantially parallel to the first plane, thereby forming a plurality of cross-points with the plurality of word lines;

wherein each memory element is disposed at one of the cross points.

16. The method of claim 15, wherein forming a distributed series diode further comprises:

forming a semi-conductor layer;

forming a material layer; and

forming a metal layer.

17. The method of claim 15, further comprising forming multiple read circuits, each read circuit being coupled to at least one bit line and operable to sense current flow through a selected memory cell.

18. The method of claim 17, wherein each read circuit comprises a differential amplifier.

19. The method of claim 18, wherein the differential amplifier is operable to compare current flowing through a selected memory cell with current flowing through at least one reference cell.

20. The method of claim 19, further comprising forming an equipotential generator coupled to the word lines and the bit lines and operable to set voltage levels in the memory device to prevent parasitic currents from flowing through unselected memory cells.

21. A data storage device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of cross points formed by the word lines and the bit lines;

a plurality of memory cells, each of the memory cells being located at a different one of the cross points; and

a first bit line comprising a distributed series diode with a metal layer, a semiconductor layer, and a material layer disposed between the metal layer and the semiconductor layer, the distributed series diode extending along an entire length of the bit line such that each of the associated memory cells located along the first bit line is coupled between the distributed series diode and an associated word line.

22. The data storage device of claim 21, wherein each of the bit lines comprises a distributed series diode.

23. The data storage device of claim 22, wherein the distributed series diode isolates a first group of memory elements from other memory elements along the first bit line.

24. A method for forming a data storage device, comprising:

forming a plurality of word lines;

forming a plurality of memory elements on the plurality of word lines;

forming at least one distributed series diode; and

forming a plurality of cross-points with a plurality of word lines;

wherein each memory element is disposed at one of the cross points and the at least one distributed series diode is adjacent to one of the plurality of bit lines.

25. The method of claim 24, wherein forming a distributed series diode further comprises:

forming a semi-conductor layer;

forming a material layer; and

forming a metal layer.

26. The method of claim 24, wherein forming a distributed series diode further comprises forming a distributed series diode adjacent each bit line.